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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,830	01/30/2001	Frank K. Baker JR.	SC11150TH	2027

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EXAMINER	
NAMAZI, MEHDI	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/772,830	Applicant(s) BAKER ET AL.	
	Examiner Mehdi Namazi	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-10 and 12-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15* is/are allowed.

6)☒ Claim(s) *1-4, 6-10, 12-14, and 16-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to amendment filed April 29, 2004.

Response to Arguments

1. Applicant's arguments with respect to claims 1-4, 6-10, 12-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6-10, 12-14, 16-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno (US. Patent 6,105,114), and further in view of Cliff et al. (6,392,438).

As per claim 1, 6, and 16, Okuno teaches a memory system comprising: an array of addressable storage elements arranged in a plurality of rows and a plurality of columns (fig. 9); and decoding circuitry coupled to the array of addressable storage elements (fig. 5), the decoding circuitry, responsive to decoding a first address, to access a first storage element of a first row of the plurality of rows, and the decoding circuitry, responsive to decoding a second address consecutive to the first address, to access a second storage element of a second row of the plurality of rows

(fig. 8A shows accessing first and second row consecutively, the second row of the plurality of rows different from the first row of the plurality of row (fig. 9 shows first row is different from second row); wherein the first address comprises a group of bits (inherent, because any address is comprising of plurality of bits); wherein the second address comprises a group of bits (inherent, because any address is comprising of plurality of bits); wherein the decoding circuitry includes a row decoder and a column decoder (fig. 5elements 3, and 4); wherein the row decoder is operable responsive to a first portion of the group of bits of the first address and the second address (fig. 11 A); wherein the column decoder is operable responsive to a second portion of the group of bits of the first address and the second address (fig. 11B), wherein a bit of the second portion is more significant than a bit of the first portion (cols. 7-8, lines 65-8).

As per claims 14, 22, and 25 Okuno teaches an embedded control system comprising: a processor (it is inherent for any system to have a processor which has not been shown here); and a memory system coupled to the processor (fig. 5), the memory system comprising an input to receive an address signal from the processor (fig. 5, "address signal ADR"), an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks

comprising: an array of memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages (fig. 9), each of the plurality of pages comprising a plurality of words (inherent), each of the plurality of words comprising a plurality of bits (inherent); and decoding circuitry comprising a column decoder and a row decoder (fig. 1, elements 3, and 4), the decoding circuitry coupled to the input, the output and the array of memory cells (fig. 5), the decoding circuitry, responsive to the address signal having a first address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second address consecutive to the first address, accessing a seconds page of a second row of the plurality of rows, and, thereafter (fig. 8A shows accessing first and second and .....rows), the decoding circuitry coupling the first and second pages to the output (accessing first row as page address and second row as second page); wherein the address signal comprises a group of bits (inherent); the row decoder is operable responsive to a first portion of the group of bits; the column decoder is operable responsive to a second portion of the group of the bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion (cols. 7-8, lines 65-8).

As per claims 1, 6, 16, 14, 22, and 25, Okuno teaches the claimed invention as detailed above in the previous paragraph, but fails to teach a storage with plurality of nonvolatile memory cells.

Cliff similarly discloses a storage with plurality of memory cell array, wherein data could be read or written as a ROM array. In this way Cliff teaches a storage with plurality of nonvolatile memory cells, in order to preserved data from erasure.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to use a nonvolatile memory, wherein nonvolatile memory is able to conserve data even when there is no power supply, as taught by Cliff into system of Okuno in order to preserve data from erasure in case of power shortage. One ordinary skill in the art would found ample suggestion therein to modify the Okuno system by providing a plurality of nonvolatile memory cells, where each memory cell can preserve one bit of data in event of power failure.

As per claims 2, 8, Okuno teaches wherein each of the storage elements stores one bit (it is inherent for each cell to store at least one bit of data).

As per claims 3, 9, Okuno teaches wherein each of the storage elements stores a plurality of bits arranged as a word (fig. 9, any few cells together could create a word).

As per claims 4, 10, Okuno teaches wherein each of the storage elements stores a plurality of bits arranged as a page (fig. 9, each row is comprising a plurality of bits to create a page).

As per claim 7, Okuno teaches wherein:

a) the input of each of the storage elements is a control gate, and

b) the output of each of the storage elements is a drain (fig. 13).

As per claim 12, Okuno teaches wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell (it is inherent to use floating gate to detect the threshold voltage states in the cell transistor).

As per claim 13, Okuno teaches wherein the at least one of the less significant bits comprises all of the less significant bits (col. 8, lines 1-8).

As per claim 17, Okuno teaches wherein accessing a first storage element comprises reading a first page, the first page comprising a plurality of bits (it is inherent to consider first row as first element, wherein each row is comprising a plurality of bits to create a page).

As per claim 18, Okuno teaches wherein accessing a second storage element comprises reading a second page different from the first page, the second page comprising a plurality of bits (it is inherent to consider second row as second element, wherein each row is comprising a plurality of bits to create a second page).

As per claim 19, Okuno teaches wherein accessing a first storage element comprises initiating a first burst access, the first burst access comprising a plurality of bits (it is inherent to access first row as a first burst).

As per claim 20, Okuno teaches wherein accessing a second storage element comprises initiating a second burst access different from the first burst access, the second burst access comprising a plurality of bits (it is inherent to access the second row as a second burst).

As per claim 21, Okuno teaches wherein: the numeric address comprises a group of bits (inherent); the row decoder is operable responsive to a first portion of the group of bits; the column decoder is operable responsive to a second portion of the group of bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion (cols. 7-8, lines 65-8).

As per claims 23, and 24 Okuno teaches wherein the at least one of the less significant bits comprises all of the less significant bits (col. 8, lines 1-8).

Allowable Subject Matter

4. Claim 15 is allowed.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 703-306-2758. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mehdi Namazi
Examiner
Art Unit 2188

July 9, 2004

Mano Padmanabhan 7/12/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER